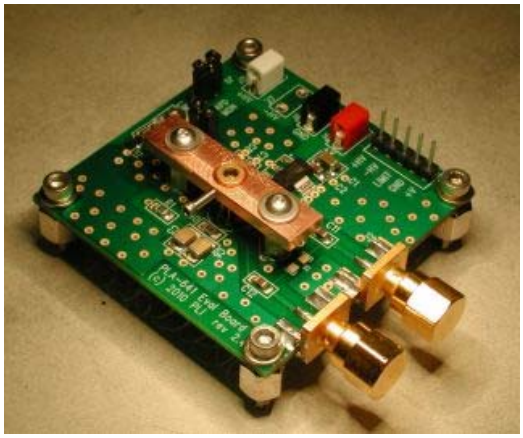
PLA-641 – High Sensitivity APD Receiver Evaluation Board

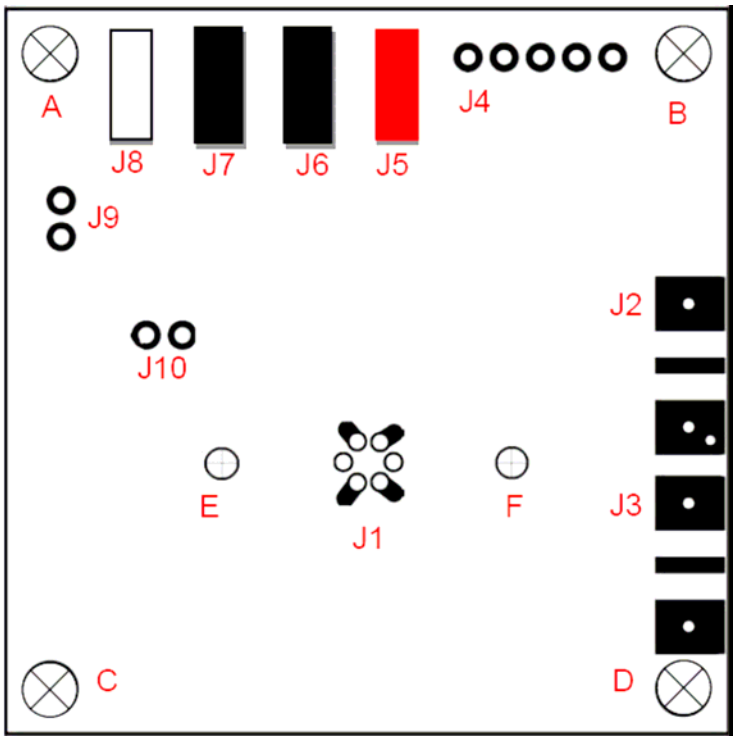
Product Features

- Evaluation of PLA641
- Mechanical features for mounting of focusing optics and/or panel mounting for range testing
- Onboard suppression power supply transients and ripple



The evaluation board provides basic I/O access to the PLA-641 High Sensitivity APD Front End Receiver Modules. The evaluation board provides some transient and ripple-rejection of the input bias with on-board filtering and linear voltage regulation.

1. BOARD OUTLINE



Location (inches)*

Hole	X	Y
A (1/4")	-0.875	1.125
B (1/4")	0.875	1.125
C (1/4")	-0.875	-0.625
D (1/4")	0.875	-0.625
E (0.086")	-0.4	0
F (0.086")	0.4	0

* Reference to DUT

Evaluation Board Outline (2in x 2in).

2. JUMPERS

JUMPER	Function	TYPE
J2	SIGNAL (+, AC coupled)	SMA
J3	SIGNAL (-, AC coupled)	SMA
J4*	Alternate power and signal	5-PIN HEADER
J5	+V	MINI BANANA
J6	GND	MINI BANANA
J7	HV (-)	MINI BANANA
J8	HV (+)	MINI BANANA
J9	APD current monitor	2-PIN HEADER
J10	Limiter diode current monito	2-PIN HEADER

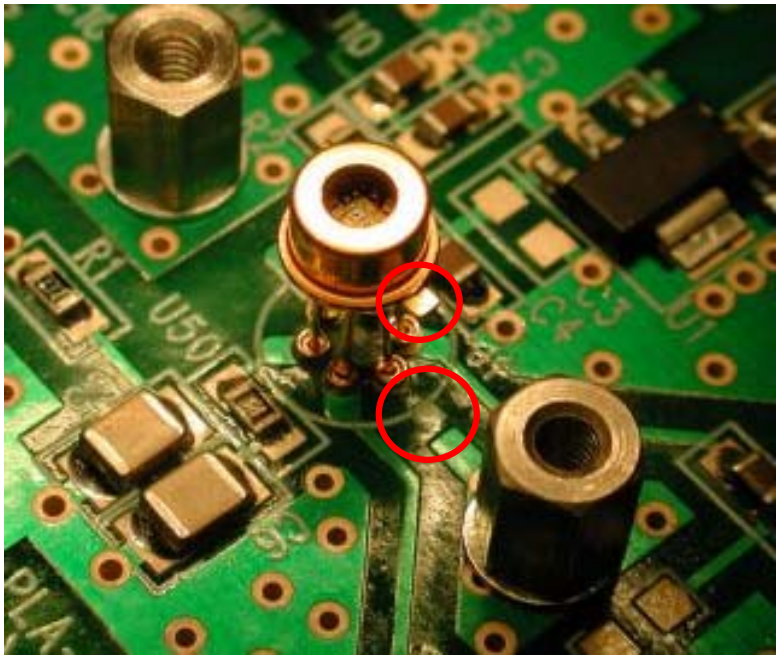
* Redundant I/O

J4 Pins	Function
1	+V
2	GND
3	LIMITER
4	HV-
5	HV+

NOTE: Jumpers J4 provide alternate, redundant methods of I/O for signal and power. For inputs (e.g. +V, +HV, etc.), only one method should be used at a time.

3. MODULE INSERTION

The tab of the TO46 header should point directly towards the SMA output connectors, and aligned with the silkscreen on the PCB.



The full lead length may be used without penalty to the intrinsic performance of the receiver (noise or bandwidth), but if excessive RFI is observed at the output of the TIA, trimming the leads should be considered.

4. THERMAL MANAGEMENT

A copper block is provided with the evaluation board. It is intended for both mechanical and thermal stabilization of the device; however, it is not intended to achieve temperature equal to ambient conditions. The critical performance (noise or bandwidth) of the receiver is not

significantly affected by the modest elevation of the base temperature. Nevertheless, the optimal bias point of the APD will shift with device temperature. Therefore, for stable operation of the receiver in this evaluation board, the receiver should be allowed to warm up for a few minutes. Alternatively, additional thermal sink should be provided to keep device temperature close to ambient.

5. INPUTS

WARNING: F*or high-sensitivity operation, care should always be taken to operate the module in a low RF noise environment. Additionally, properly shield and/or twisted pair wiring should be used for all inputs and outputs.*

Input/Output	Function
+V, GND	4.5—20V, >50mA power supply for operation of TIA. For low-noise operation, care should be used to minimize RF interference and ripple in the power supply and cable. The evaluation board includes noise filtering and linear voltage regulator that converts the evaluation board power supply to the appropriate +3.3V to operate the TIA. About 1mA of the +V supply is used by the evaluation board, and the remaining current draw is used by the TIA. Power supply voltage may be applied either to J4 or to J5+J6, but both should not be used simultaneously.
HV+, HV-	The high voltage bias (up to +65V) applied across the HV+ (J8 or J4.5) and HV- pins (J7 or J4.4) for reverse-bias of the APD. Under small-signal operation, <1mA of current is required. For low-noise operation, care should be used to minimize RF interference and ripple in the HV supply. The evaluation board includes some by-pass capacitance for noise filtering and will present some leakage (up to 10nA) in addition to any APD dark current. HV– is tied to GND plane of the evaluation board, and HV+ is connected to the APD cathode for proper reverse-biased operation.
LIMITER	Cathode voltage of the limiter diode. The evaluation board generates the LIMITER voltage via a trim-potentiometer. Under normal operation, the header pin (J4.3) may be used only for monitoring. Alternatively, a low-impedance voltage source may be used to override the voltage generated on-board. A break-out header (J10) is allow provided on the board to monitor the average current into and out of the limiter pin of the receiver. For low-noise operation, care should be used to minimize RF interference and ripple on the LIMITER I/O.
APD BIAS MONITOR	The APD BIAS MONITOR is a 2-pin header (J9) that ties the HV– terminal of the APD bias to the board GND plane. During normal operation, a jumper of any resistance upto 10s kOhm must be used. A short-circuit jumper is included with the evaluation board, but it can be replaced by a nanometer to monitor the average APD current. The common-mode voltage of this jumper is nearly 0V above the GND plane, so there is no special requirement for isolation between the nanometer and TIA power supply. Some of the leakage current of the evaluation board will be detected in the APD BIAS MONITOR.
SIGNAL+, SIGNAL-	The differential output of the TIAs is AC-coupled (1uF) to board-edge SMA connectors (J2 and J3). The low-frequency cutoff, into a 50-ohm load, is 1.6kHz.

6. ABSOLUTE MAXIMUM RATING

WARNING: Maximum rating is of evaluation board PCB and components alone. Evaluation board specification does NOT supersede maximum rating of APD receiver module.

Parameter	Min	Max	
Supply Voltage (+V)	-0.5	16	Volt
High voltage (+HV)	-200	200	Volt
Limiter Voltage	-0.5	16	Volt
TIA Output Voltage	-16	16	Volt
TEC Voltage	-100	100	Volt
TEC Current		2.5	Amp

7. APPLICATION NOTES

Limiter Voltage

The APD receiver module requires a voltage to be applied to the cathode of the limiter diode. It is typically around 0.9V. The pin is connected to jump pin J8.3 through a 390-Ω resistor. If no bias is applied to J8.3, then the limiter voltage is pulled-up, through a 1-kΩ resistor, by a 12-turn trim-potentiometer and buffer amplifier on the evaluation board. Before the APD receiver is set in the evaluation board, the limit voltage (i.e. Vlimit, on J8.3) should be verified to be equal or slightly higher than the "LIMITER, ZERO-BIAS VOLTAGE" specified in the module test report. By virtue of the total series resistance between the buffer and the APD receiver, no significant damage should be possible by incorrectly setting the Vlimit, but the receiver performance will be affected. When Vlimit is set lower than the zero-bias voltage, the limiter diode may pull down the quiescent voltage of the TIA input. If the zero-bias voltage is too high, the effectiveness of the limiter diode to clamp in input voltage of the TIA will be diminished. Additionally, the reverse bias leakage of the limiting diode will impose a slight DC offset to the output. This will have negligible impact on the noise, but will reduce the dynamic range.

An alternative to applying a bias is to completely remove the pull-up resistor and allowing the Vlimit voltage to naturally float to the "ZERO-BIAS" condition. Under normal use, with only occasional input overload conditions, the natural quiescent point for Vlimit is the zero-bias voltage. However, under a repeating (>100 Hz) input overload condition, the value of Vlimit will drift away from zero-bias state and the effectiveness of the input limiter will be diminished.

Power Supply Ripple Rejection

To achieve maximum low-noise performance and minimize risk of damage to the receiver by power-up transients, the evaluation board is designed with a high level of broadband, power-supply ripple rejection. This is achieved, simply, with a modest RC circuit on all the power supply and bias voltage ports. Under small-signal input conditions, quiescent current

is sufficiently small that IR drop in the resistors is negligible (sub-microvolt). On the other hand, under high optical illumination (overload) condition, the APD and limiter diode biases may be shifted from quiescent by the high photocurrent. The bias will recover within a few milliseconds and the small shift in bias voltage (APD or limiter), in itself, will not significantly affect the receiver performance. However, under a repeating input overload test condition, the pulse repetition frequency should be kept low enough (<1kHz) to avoid altering the APD and limiter quiescent by an accumulative effect.

TIA output overload protection

The APD receiver includes a Schottky diode, at the TIA input, in order to shunt away excess photocurrent under overload illumination conditions. This protects the TIA from damage and improved recovery time of the TIA input stage; however, in order to enable maximum linearity and output swing, no protection is included in the APD receiver at the output of the TIA. Nevertheless, for normal use that does not require maximum output swings, it is recommended that Schottky diodes be included, external to the APD receiver module, in order to clamp the TIA output voltage swing to a maximum of 200mV and improving recovery time of the TIA output stage from input overload. Two recommended configurations are shown below: